ABSTRACT OF THE DISCLOSURE

Disclosed is a method, system and computer program product to specify an integrated circuit. The integrated circuit includes a hardwired specific logic technology portion and a programmable specific logic technology portion. The method includes generating a hybrid logic network by mapping each uncertain logic function to an abstract programmable logic element implementation thereof and by mapping each known logic function to a technology-independent logic element implementation thereof; simplifying the hybrid logic network using logic synthesis optimizations; mapping the simplified hybrid logic network to a specific technology by mapping the abstract programmable logic element implementation to the specific programmable logic technology and the technology-independent logic element implementation to the specific logic technology; and further includes optimizing the mapped network to meet performance constraints. Generating involves using integrated circuit specification language extensions that include an Uncertain Function that is used in place of a logic function or operator, an Uncertain Function Assertion for imposing at least one constraint on the Uncertain Function, an Uncertain Register for a register having a programmable size within a specified range and an Uncertain Constant.